AMENDMENTS TO THE CLAIMS

1. (currently amended) An integrated circuit device comprising:

an array of flash memory cells, said cells comprising a source, a drain and a stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer, wherein a region under said stacked gate structure ~~is manufactured such that said region~~ comprises overlapping lateral diffusions of implantation regions of said source and said drain;

a common source line coupled with said source; and

a source contact disposed outside of said common source line and coupled with said source, wherein said source contact is coupled to said common source line under said stacked gate structure, and wherein said source contact is disposed in a row with drain contacts.

2. (original) The integrated circuit device of Claim 1 comprising substantially straight word lines.

3. (original) The integrated circuit device of Claim 1 wherein said common source line has a substantially uniform width within said array of cells.

4. (canceled)

5. (canceled)

6. (original) The integrated circuit device of Claim 1 wherein said integrated circuit device comprises a non-volatile memory.

7. (currently amended) The integrated circuit device of Claim 6 wherein said ~~non-volatile memory comprises~~ charge trapping layer is a floating gate ~~as a charge storage element~~.

8. (currently amended) An integrated circuit device ~~wherein parameters comprising dopant species, dopant concentration, implant energy, temperature, and duration are controlled during manufacture such that said manufacture achieves~~ comprising a first non-volatile flash memory cell comprising:

a first stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer; and

a first region under ~~a~~ said first stacked gate structure ~~that comprises~~ comprising overlapping lateral diffusions of source and drain implantation regions.

9. (original) The integrated circuit device of Claim 8 wherein one of said implantation regions is coupled to a first source contact.

10. (original) The integrated circuit device of Claim 8 wherein one of said implantation regions is coupled to a common source line.

11. (currently amended) The integrated circuit device of Claim 8 further comprising a second non-volatile flash memory cell comprising a second stacked gate structure comprising a control gate, a charge trapping layer and an insulating layer, wherein ~~parameters comprising dopant species, dopant concentration, implant energy, temperature, and duration are controlled during manufacture such that said manufacture~~

~~achieves~~ a second region under said second stacked gate structure comprises overlapping lateral diffusions of source and drain implantation regions.

12. (currently amended) The integrated circuit device of Claim 11 wherein one of said implantation regions associated with said second stacked gate structure is coupled to a second source contact.

13. (original) The integrated circuit device of Claim 11 wherein one of said implantation regions associated with said second gate structure is coupled to said common source line.

14. (canceled)

15-20. (cancelled)